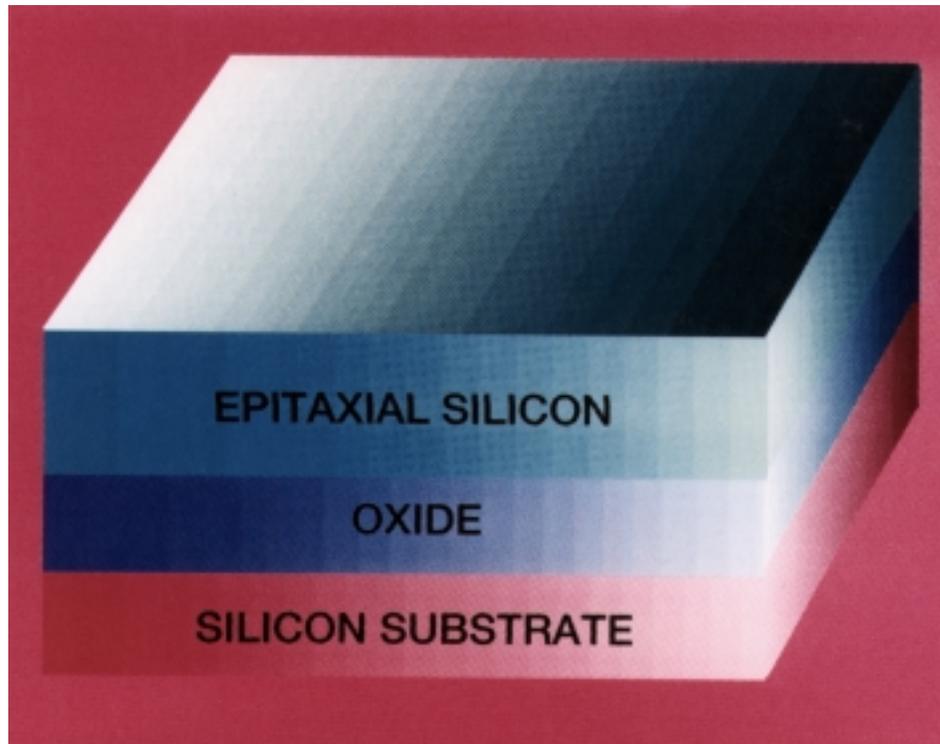


ADVANCED SILICON-ON-INSULATOR TECHNOLOGY



It is projected that by the year 2000, high-performance VLSI technologies will use silicon-on-insulator (SOI) substrate wafers. Bond-and-etchback SOI (BESOI) is one of the leading candidate technologies for low-cost, high-quality SOI wafers. Other important application areas for SOI technologies are power devices and military electronics. The Naval Research Laboratory (NRL) has patented and demonstrated a BESOI process using a silicon-germanium (Si-Ge) etch stop rather than the conventional boron doping layer etch stop. The advantages of the Si-Ge etch stop approach are

- The Si-Ge BESOI process is free from boron incorporation.
- The active silicon layer is free from dislocations and electrically active impurities.
- Thin silicon layer thicknesses are easily obtainable. (NRL has demonstrated that 200 nm thick SOI layers and <100 nm layers are easily obtainable.)
- The Si-Ge BESOI technology allows oxide radiation hardening techniques to be incorporated into the buried oxide. (Significantly smaller radiation induced shifts are observed in Si-Ge BESOI compared to SIMOX.)
- The invention includes the case of combining a boron etch stop with a Si-Ge etch stop to achieve high selectivity without boron incorporation.

This patented BESOI technology is available for license; cooperative research and development agreements (CDRAs) in this technology area are also possible. It is envisioned that this patent would be important in establishing a position as a SOI wafer supplier to the VLSI industry.

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